ISO9001:2000 Certified SCI Quality System

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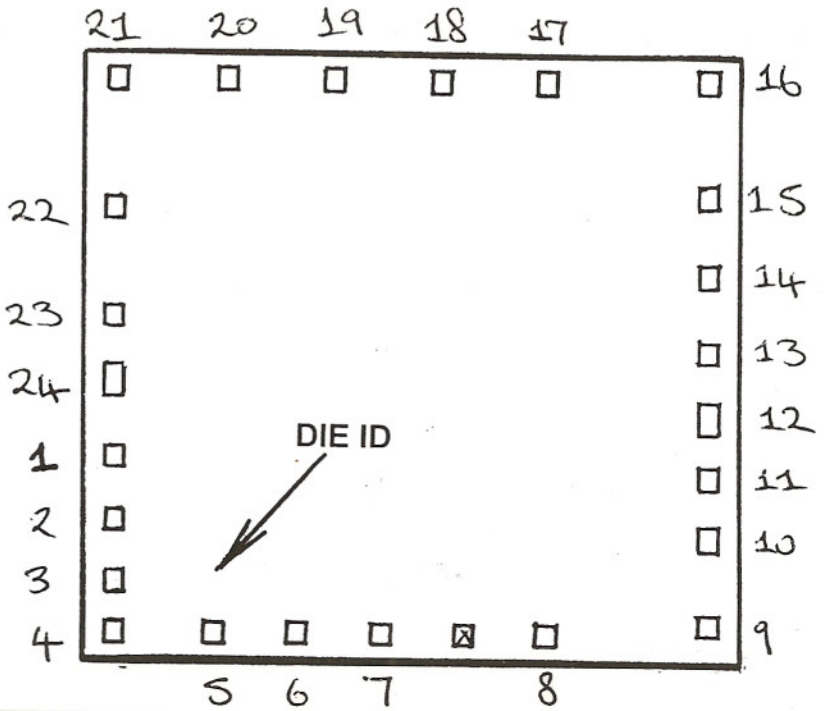
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

Pad	Function
1	$\overline{CS}$
2	$\overline{RD}$
3	$\overline{WR}$
4	A0
5	A1
6	A2
7	A3
8	A4
9	V_{BB}
10	OSC IN
11	OSC OUT
12	GND
13	MFO
14	$\overline{INTR}$
15	D0
16	D1
17	D2
18	D3
19	D4
20	D5
21	D6
22	D7
23	$\overline{PFAIL}$
24	V_{CC}



Topside Metal: Al
Backside: Si
Backside Potential: -
Mask Ref: B
Bond Pads: .004" x .004"

APPROVED BY: CD	**DIE SIZE: .156" x .136"**	**DATE: 7/23/02**
MFG: National	**THICKNESS: .015"**	**P/N: DP8572**